25-Jul-94
Test Procedure for the Rhic Real Time Data Link Input Board
Schematic #94028014

Equipment Used: Fluke hand held Digital Multimeter
2 Channel Oscilloscope
2 Oscilloscope Probes
Logic Analyzer
Real time Timing System
Pulse Generator (up to 10KHz)
2 BNC terminated coax cables
Dumb Terminal
6U VME Extender Board
MVME167 Processor Board with monitor proms installed
Rhic Real Time Data Link Encoder Board #94028013
Rhic Real Time Data Link Test Boards

I. General Inspection and Set-up

1.) Before applying power to the board:
a. check all IC's for proper insertion (no bent under pins), proper device type and orientation.
b. check for proper polarity on electrolytic capacitors.
c. check for shorts from +5 to ground with ohm meter.
d. check all values on analog parts, resistors, capacitors, etc.
e. check resistor sips for proper orientation and value.
f. check for solder bridges on connectors and pin grid arrays.
g. check for proper orientation of sip delay line.

2.) Program all programmable devices: (hartmann\altera\rtdl)
a. U1 - EPM5130 Filename 94028015.gdf (\inpbd4.0\vmeintfc.gdf)
b. U16 - EPM7128GC-4 Filename 94028016.gdf (\inpbd4.0\serlnk\sertrndc.gdf)
c. U76 - EPM7128GC-4 Filename 94028016.gdf (\inpbd4.0\serlnk\sertrndc.gdf)
d. U8 - 82S123 Filename 94028018.hex (hartmann\pld\rhic\statid1.hex)

94028018 (Statid1.hex) must be modified individually for each board to include the major revision level, the minor revision level and the board serial number.

3.) Power board on. Check +5 to ground at different points around the board. Make sure all points are >= 4.75 and <= 5.25. Power board off.

4.) Insert all programmable IC's into the proper sockets, checking for proper orientation and proper insertion.

5.) Jumper the board for the proper Parameter ID for each channel, Type Field for each channel and VME base address.

II. VME Test

1.) Connect the terminal to the front panel db25 connector on the MVME162 processor board.

2.) Power on chassis and terminal.

3.) Processor should prompt with '->'.
This board occupies 256 bytes of memory space. This memory space consists of the status/id bytes (64) (read only), the command registers (2)

(read/write), the status/interrupt status registers (2) (read only), the Device Data Registers (2-32 bit) (read only), the VME Data Register (2-32 bit) (read/write) and the interrupt vector register (read/write). The upper 8-bits of the address are jumper selectable. Type at the prompt 'd 0xffffxx00'. This command will Display the first 256 bytes of memory at the base address xxh.
The first 64 bytes are the VME ID and board related information. This data is configured as '2E' (ASCII period) in all even locations, and data (ASCII text) in all odd locations. Display should show:

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ffffxx00      2E56 2E4D 2E45 2E49 2E44 2E42 2E4E 2E4C   .V.M.E.I.D.B.N.L
ffffxx10      2E56 2E31 2E30 2E36 2Exx 2Exx 2Exx 2Exx   .V.1.0.6.x.x.x.x
ffffxx20      2Exx 2Exx 2Exx 2Exx 2Exx 2Exx 2Exx 2Exx   .x.x.x.x.x.x.x.x
ffffxx30      2Exx 2Exx 2Exx 2Exx 2Exx 2Exx 2Exx 2Exx   .x.x.x.x.x.x.x.x
ffffxx40      xx00 xx00 xxxx FFxx xxxx FFxx xxxx FFxx   ................
ffffxx50      xxxx FFxx FF00 xxxx xxxx FFFF FFFF FFFF   ................
ffffxx60      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffffxx70      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffffxx80      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffffxx90      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffffxxA0      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffffxxB0      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffffxxC0      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffffxxD0      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffffxxE0      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffffxxF0      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
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4.) The Command Register is located at address ffffxx40 (ffffxx42). Verify that the data at ffffxx40 (ffffxx42) is xx00. Each of the low order 8 bits should be toggled on and off to verify writing to and reading from that register. To write bit 0, at the prompt type 'm 0xffff0040^'. Monitor should respond with 'ffffxx40 - ' ('ffffxx42 -'). Type in '0001'. This should set bit 0. To stop the write operation type '.^'. To read bit 0, type 'd 0xffffx040'. Verify that bit 0 was set. All other low order bits (0-7) should be set in this way. Once all of the command bits have been checked, write a '0000' to the command register. Verify its contents.

5.) The Status/Interrupt Status Register is a 16 bit register located at address ffffxx56 (ffffxx58). The upper 8 bits are the Parameter ID. Verify that the contents of the lower 8 bits of this register correspond to the current status/Interrupt Status of the board.

6.) The VME Data Register is located at ffffxx44 (ffffxx48), and is 24 bits. The Most Significant Byte is located at ffffxx47 (ffffxx4b) . Verify that these registers can be written and then verify that the contents contain the data that was loaded.

7.) The Interrupt Vector Register is an 8-bit register located at address ffffxx54. Set the contents of this register to 40H. Verify that this location contains 40H.

8.) To test interrupt capabilities, the processor needs to be initialized. To connect the interrupt, type intConnect (4 * 40, logMsg, "Interrupt Generated\n"). This will print "Interrupt Generated" whenever interrupt #40 occurs. (The Vector). Type sysIntEnable (1). This command will handle VMEbus level 1 interrupt. Set the Command register to a 28H. This will set the interrupt generated to a level 1 interrupt and enable the interrupt. Check all interrupt levels: 1 - 7 .
To generate an interrupt, remove the fiber optic connection from the test fixture.

III. General Functionality Test

1.) The Device Data Registers are loaded via the front panel ST-type Fiber Optic connectors using the RTDL Waveform Generator Test Fixture. Set the dip switches for the desired parameter data and push the SETPTLD pushbutton. The 8-bit type field is fixed. Connect a pulse generator to the Transmit Trigger Input with a pulse width of 1us and frequency of no more than 10KHz. Jumper E65-E68 (E87-E90) to decode the frame sent from the test fixture. (011 = Programmed I) Connect a fiber optic pigtail between the test fixture and the RTDL IN CH1 (CH2) of the Input Module. Verify that the RTDL IN CH1 (CH2) led is lit. The Device Data Registers are located in memory at ffffxx4c (ffffxx50). The Most Significant Byte is located at ffffxx4f (ffffxx53). Verify that these registers contain the parameter data that was sent from the test fixture.

2.) Connect the logic analyzer to U74 (U81), U42 (U62), and U43 (U63) pins 2-9. Connect the clock pod to U9-8 (CLK20M).
a. Set the Mode bit in the command register(s) to a '0'. Verify that the data is the parameter data sent from the test fixture.
b. Set the Mode bit in the command register(s) to a '1'. Verify that the data is the data that was loaded into the VME Data Registers previously.

IV. General System Test

1.) Power chassis down. Plug a tested Rhic Real Time Data Link Encoder Board, Schematic #94028014 into the VME backplane. Verify that the VME base address is different from the Input Board's base address. Power up chassis. Configure the Encoder Board as per the test procedure. Verify that the Parameter ID of each channel of the Input Board has been loaded into the SRAM of the Encoder Module. Set the GO bit to a '1'.

2.) Via the monitor, download a 24-bit parameter value to ffffxx44 (ffffxx48). Verify that both channels are in VME Mode.

3.) Verify that the parameter ID and data that was loaded into the VME Data Register(s) appears on the RTDL output.

4.) Following the procedure of Section III, step 1, load a 24-bit parameter value to ffffxx4c (ffffxx50). Set the Mode bit in ffffxx40 (ffffxx42) to Device Mode.

5.) Verify that the parameter ID and data that was loaded into the Data Device Register(s) appears on the RTDL output.